populating the second surface with a plurality of conductive pads;

coupling a solder ball to each of selected ones of the plurality of conductive pads;

[and]

coupling at least one semiconductor die and at least one passive device to the first surface, wherein the at least one passive device is selected from a group comprising resistors, capacitors, and inductors;

testing said at least one semiconductor die; and
coupling said interposer to a substrate after said testing if said at least one
semiconductor die passes said testing.

20. (Amended twice) The method of claim 19 wherein testing includes testing at integrated cache speeds [further comprising coupling the interposer to a substrate].

(Amended once) The method of claim 19 wherein fabricating comprises abricating the interposer with organic material.

- 22. (temporarily removed from consideration) (Amended once) The method of claim 19 wherein coupling at least one semiconductor die comprises a C4 process.
- 23. (Amended twice) The method of claim [20] 19 further comprising [testing the semiconductor dice coupled to the interposer prior to coupling the interposer to the substrate] not coupling said interposer to the substrate if said at least one semiconductor die does not pass said testing.
- 24. (temporarily removed from consideration) (Amended once) The method of claim 19 further comprising coupling a single chip carrier to the substrate.